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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> <i>( Not for submission under 37 CFR 1.99)</i>	Application Number		10675778
	Filing Date		2003-09-30
	First Named Inventor		DeWitt, Jr. et al.
	Art Unit		2183
	Examiner Name		Cody, Dillon J.
	Attorney Docket Number		AUS920030480US1

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2	4316245			1982-02-16	Luu et al.	
3	7181723			2007-02-20	Luk et al.	
4	6961925			2005-11-01	Callahan, II et al.	
5	5950003			1999-09-30	Kaneshiro et al.	
6	5212794			1993-05-18	Pettis et al.	
7	5659679			1997-08-19	Alpert et al.	
8	6006033			1999-12-21	Heisch	

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9	6119075		2000-09-12	Dean et al.	
10	6189141	B1	2001-02-13	Benitez et al.	
11	6237141	B1	2001-05-22	Holzie et al.	
12	6351844	B1	2002-02-26	Bala	
13	6505292	B1	2003-01-07	Witt	
14	6631514	B1	2003-10-07	Le	
15	5794026		1998-06-11	Tran	
16	5950009		1999-09-07	Bortnikov et al.	
17	5950003		1999-09-07	Kaneshiro et al.	
18	5581778		1996-12-03	Chin et al.	
19	5752062		1998-05-12	Gover et al.	

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	20	6446029	B1	2002-09-03	Davidson et al.	
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	1	20040194076	A1	2004-09-01	Comp et al.	
	2	20020073406	A1	2002-06-13	Gove	
	3	20030014741	A1	2003-01-16	Megiddo et al.	
	4	20020157086	A1	2002-10-24	Lewis et al.	
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	Ts
	1	RAMIREZ et al., "The Effect of Code Reordering on Branch Prediction", Proceedings of the International Conference on Parallel Architectures and Compilation Techniques, October 2000, pp. 189-198.	<input type="checkbox"/>
	2	YANG et al., "Improving Performance by Branch Reordering", Proceedings of the ACM SIGPLAN 1998 Conference on Programming Language Design and Implementation, Montreal Canada, 1008, pp. 130-141.	<input type="checkbox"/>
	3	CONTE et al., "Accurate and Practical Profile-Driven Compilation Using the Profile Buffer", Proceedings of the 29th Annual ACM/IEEE International Symposium on Microarchitecture, Paris, France, 1996, pp. 36-45.	<input type="checkbox"/>
	4	CONTE et al., "Using Branch Handling Hardware to Support Profile-Driven Optimization", Proceedings of the 27th Annual International Symposium on Microarchitecture, San Jose CA, 1994, pp. 12-21.	<input type="checkbox"/>
	5	FISHER, "Trace Scheduling: A Technique for Global Microcode Compaction", IEEE Transactions on Computers, Vol. C30, No. 7, July 1981, pp. 478-490.	<input type="checkbox"/>
	6	CHANG et al., "Using Profile Information to Assist Classic Code Optimizations", Software Pract. Exper. 21, December 1991, pp. 1301-1321.	<input type="checkbox"/>
	7	SCHMIDT et al., "Profile-Directed Restructuring of Operating System Code", IBM Systems Journal, 1998, Vol. 37, No. 2, pp. 270-297.	<input type="checkbox"/>
	8	AHO et al., "Compilers: Principles, Techniques, and Tools", Addison-Wesley, 1988, pp. 488-497.	<input type="checkbox"/>
	9	INTEL, "Intel IA-64 Architecture Software Developer's Manual", Revision 1.1, Vol. 4, No. 245320.002, July 2001.	<input type="checkbox"/>

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Signature	/Gerald H. Glanzman/	Date (YYYY-MM-DD)	2007-03-27
Name/Print	Gerald H. Glanzman	Registration Number	25,035

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